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10/566,914	03/20/2006	Masaki Onishi	19415-008US1 PCT-04R-170/	4205
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FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			ROJAS, DANIEL E	
			ART UNIT	PAPER NUMBER
			2816	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 10/566,914	Applicant(s) ONISHI ET AL.	
	Examiner DANIEL ROJAS	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 September 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,8,11-14 and 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,8,11-14 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 September 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 9/15/2008 have been fully considered but they are not persuasive. The input signals to a circuit in an apparatus claim do not define the structure over the prior art. Higuchi's circuit (Figure 6) is capable of use when the input signal "a" is equal to or connected to Ci (i.e. the state control signal).
2. Examiner confirms reception of the foreign priority document and has withdrawn the indefiniteness rejection under U.S.C. 112, second paragraph.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
5. Claims 1-8 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi et al (US Patent No. 5,053,646), hereinafter referred to as Higuchi.

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6. For claim 1, Higuchi teaches in Figure 6 a circuit which comprises a three-state inverter (comprised of 41, 42, 43, and 44) that switches the output thereof among three states, namely a high, a low, and a high-impedance state (as explained below); and an inverter (40) but fails to teach that the three-state inverter has a threshold voltage with reference to which the three-state inverter evaluates an input thereto to determine whether or not to change a state of an output thereof is equal to substantially one-half of a supply voltage fed in and that the inverter of which a threshold voltage with reference to which the inverter evaluates an input thereto to determine whether or not to change a state of an output thereof is equal to substantially one-half of the supply voltage fed in. However, it would have been obvious to one of ordinary skill in the art at the time of invention to set the threshold voltage of both the said three-state inverter and the said inverter to substantially one half of the supply voltage fed in since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Higuchi further teaches that one of the logic gates is a two-input, one-output AND gate (as explained below) comprising: a first three-state inverter (41, 42, 43, 44) of which an input terminal (a) serves as one input of the AND gate; a second three-state inverter (45, 46, 47, 48) of which an input terminal (b) serves as another input of the AND gate and of which the input terminal is connected to a state control terminal thereof (as explained below), the second three-state inverter determining whether or not to bring an output thereof into a high-impedance state according to a state of a signal fed to the state control terminal thereof (inherent based on the structure of Higuchi); a first inverter (40) of which an

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input terminal is connected to a node between output terminals of the first and second three-state inverters, and of which an output terminal serves as an output of the AND gate; and a second inverter (49) of which an input terminal is connected to the input terminal of the second three-state inverter (in parallel, as shown), and of which an output terminal is connected to the state control terminal of the first three-state inverter (gate of 44) but fails to teach that the threshold voltages of the first and second three-state inverters and of the first and second inverters are substantially equal to one-half of the supply voltage fed in. The signals being inputted to a circuit relates only to the intended use and does not distinguish the structure of a circuit over the prior art.

Therefore, Higuchi's circuit is capable of use wherein the input signal "a" is equal to the state control signal C_i . It would have been obvious to one of ordinary skill in the art at the time of invention to set the threshold voltage of both the said first and second three-state inverters and the said first and second inverters to substantially one half of the supply voltage fed in since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

7. For claim 3, the modified version of Higuchi as defined above teaches the circuit of claim 2 but fails to teach that the first inverter is a three-state inverter of which a state control terminal is grounded. However, a three state inverter of which a state control terminal is grounded operates in the same way as a push-pull inverter (i.e. a PMOS transistor with a gate connected to an input, drain connected to the output and source connected to the supply voltage and an NMOS transistor with a gate connected to the

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input, drain connected to the output and source connected to ground). Therefore, it would have been obvious to one of ordinary skill in the art to replace Higuchi's inverter with a three state inverter of which a state control terminal is grounded because the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of invention.

8. For claim 4, Higuchi teaches in Figure 6 a circuit which comprises a three-state inverter (comprised of 41, 42, 43, and 44) that switches the output thereof among three states, namely a high, a low, and a high-impedance state (as explained below); and an inverter (40) but fails to teach that the three-state inverter has a threshold voltage with reference to which the three-state inverter evaluates an input thereto to determine whether or not to change a state of an output thereof is equal to substantially one-half of a supply voltage fed in and that the inverter of which a threshold voltage with reference to which the inverter evaluates an input thereto to determine whether or not to change a state of an output thereof is equal to substantially one-half of the supply voltage fed in. However, it would have been obvious to one of ordinary skill in the art at the time of invention to set the threshold voltage of both the said three-state inverter and the said inverter to substantially one half of the supply voltage fed in since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Higuchi further teaches a two-input, one-output OR gate (as explained below) comprising: a first three-state inverter of which an input terminal serves as one input of the OR gate (a), and that receives at a state control terminal thereof another input to the OR gate (c_i), the first

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three-state inverter determining whether or not to bring an output thereof into a high-impedance state according to a state of a signal fed to the state control terminal thereof (inherent based on the structure of Higuchi, as further defined below); a second three-state inverter of which an input terminal serves as another input of the OR gate (b); a first inverter (40) of which an input terminal is connected to a node between output terminals of the first and second three-state inverters, and of which an output terminal serves as an output of the OR gate; and a second inverter (49) of which an input terminal is connected to the input terminal of the second three-state inverter (since they are receiving the same signal, they are inherently electrically connected, as further explained below), and of which an output terminal is connected to the state control terminal of the second three-state inverter (as shown), but fails to teach that the threshold voltages of the first and second three-state inverters and of the first and second inverters are substantially equal to one-half of the supply voltage fed in. A three input, one output OR gate inherently comprises two inputs and one output. The signals being inputted to a circuit relates only to the intended use and does not distinguish the structure of a circuit over the prior art. Therefore, Higuchi's circuit is capable of use wherein the input signal "a" is equal to the state control signal C_i . It would have been obvious to one of ordinary skill in the art at the time of invention to set the threshold voltage of both the said first and second three-state inverters and the said first and second inverters to substantially one half of the supply voltage fed in since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

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9. For claim 5, the modified version of Higuchi as defined above teaches the circuit of claim 4 but fails to teach that the first inverter is a three-state inverter of which a state control terminal is grounded. However, a three state inverter of which a state control terminal is grounded operates in the same way as a push-pull inverter (i.e. a PMOS transistor with a gate connected to an input, drain connected to the output and source connected to the supply voltage and an NMOS transistor with a gate connected to the input, drain connected to the output and source connected to ground). Therefore, it would have been obvious to one of ordinary skill in the art to replace Higuchi's inverter with a three state inverter of which a state control terminal is grounded because the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of invention.

10. For claim 8, Higuchi further teaches that the three-state inverter comprises: a first transistor (42) that receives at a first electrode thereof the supply voltage (source terminal via transistor 41); a second transistor (41) of which a first electrode (source terminal) is connected to a second electrode (drain terminal, via the source) of the first transistor, and that is of a same conductivity type as the first transistor (PMOS, as shown); a third transistor (44) of which a second electrode (drain terminal) is connected to a second electrode of the second transistor (drain terminal), and that is of an opposite conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of which a second electrode (drain terminal) is connected to a first electrode (source terminal) of the third transistor, of which a first electrode is grounded (via transistor 44), and that is of an opposite conductivity type to the first transistor (NMOS); and an

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inverter (49) of which an output terminal is connected to a control electrode of the third transistor (44), wherein a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter (terminal at which a is applied), a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter (the node connected to the input of 40), and a node between a control electrode of the second transistor and an input terminal of the inverter serves as a state control terminal of the three-state inverter (as shown).

11. For claim 11, the modified version of Higuchi as defined above teaches a first transistor (42) that receives at a first electrode thereof the supply voltage (source terminal via transistor 41); a second transistor (41) of which a first electrode (source terminal) is connected to a second electrode (drain terminal, via the source) of the first transistor, and that is of a same conductivity type as the first transistor (PMOS, as shown); a third transistor (44) of which a second electrode (drain terminal) is connected to a second electrode of the second transistor (drain terminal), and that is of an opposite conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of which a second electrode (drain terminal) is connected to a first electrode (source terminal) of the third transistor, of which a first electrode is grounded (via transistor 44), and that is of an opposite conductivity type to the first transistor (NMOS); and an inverter (49) of which an output terminal is connected to a control electrode of the third transistor (44), wherein a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter (terminal at which a is

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applied), a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter (the node connected to the input of 40), and a node between a control electrode of the second transistor and an input terminal of the inverter serves as a state control terminal of the three-state inverter (as shown).

12. For claim 12, the modified version of Higuchi as defined above teaches a first transistor (42) that receives at a first electrode thereof the supply voltage (source terminal via transistor 41); a second transistor (41) of which a first electrode (source terminal) is connected to a second electrode (drain terminal, via the source) of the first transistor, and that is of a same conductivity type as the first transistor (PMOS, as shown); a third transistor (44) of which a second electrode (drain terminal) is connected to a second electrode of the second transistor (drain terminal), and that is of an opposite conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of which a second electrode (drain terminal) is connected to a first electrode (source terminal) of the third transistor, of which a first electrode is grounded (via transistor 44), and that is of an opposite conductivity type to the first transistor (NMOS); and an inverter (49) of which an output terminal is connected to a control electrode of the third transistor (44), wherein a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter (terminal at which a is applied), a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter (the node connected to the input of 40), and a node between a control electrode of the second transistor and an input

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terminal of the inverter serves as a state control terminal of the three-state inverter (as shown).

13. For claim 13, the modified version of Higuchi as defined above teaches a first transistor (42) that receives at a first electrode thereof the supply voltage (source terminal via transistor 41); a second transistor (41) of which a first electrode (source terminal) is connected to a second electrode (drain terminal, via the source) of the first transistor, and that is of a same conductivity type as the first transistor (PMOS, as shown); a third transistor (44) of which a second electrode (drain terminal) is connected to a second electrode of the second transistor (drain terminal), and that is of an opposite conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of which a second electrode (drain terminal) is connected to a first electrode (source terminal) of the third transistor, of which a first electrode is grounded (via transistor 44), and that is of an opposite conductivity type to the first transistor (NMOS); and an inverter (49) of which an output terminal is connected to a control electrode of the third transistor (44), wherein a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter (terminal at which a is applied), a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter (the node connected to the input of 40), and a node between a control electrode of the second transistor and an input terminal of the inverter serves as a state control terminal of the three-state inverter (as shown).

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14. For claim 14, the modified version of Higuchi as defined above teaches a first transistor (42) that receives at a first electrode thereof the supply voltage (source terminal via transistor 41); a second transistor (41) of which a first electrode (source terminal) is connected to a second electrode (drain terminal, via the source) of the first transistor, and that is of a same conductivity type as the first transistor (PMOS, as shown); a third transistor (44) of which a second electrode (drain terminal) is connected to a second electrode of the second transistor (drain terminal), and that is of an opposite conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of which a second electrode (drain terminal) is connected to a first electrode (source terminal) of the third transistor, of which a first electrode is grounded (via transistor 44), and that is of an opposite conductivity type to the first transistor (NMOS); and an inverter (49) of which an output terminal is connected to a control electrode of the third transistor (44), wherein a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter (terminal at which a is applied), a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter (the node connected to the input of 40), and a node between a control electrode of the second transistor and an input terminal of the inverter serves as a state control terminal of the three-state inverter (as shown).

15. For claim 16, the modified version of Higuchi as defined above teaches a first transistor (42) that receives at a first electrode thereof the supply voltage (source terminal via transistor 41); a second transistor (41) of which a first electrode (source

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terminal) is connected to a second electrode (drain terminal, via the source) of the first transistor, and that is of a same conductivity type as the first transistor (PMOS, as shown); a third transistor (44) of which a second electrode (drain terminal) is connected to a second electrode of the second transistor (drain terminal), and that is of an opposite conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of which a second electrode (drain terminal) is connected to a first electrode (source terminal) of the third transistor, of which a first electrode is grounded (via transistor 44), and that is of an opposite conductivity type to the first transistor (NMOS); and an inverter (49) of which an output terminal is connected to a control electrode of the third transistor (44), wherein a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter (terminal at which a is applied), a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter (the node connected to the input of 40), and a node between a control electrode of the second transistor and an input terminal of the inverter serves as a state control terminal of the three-state inverter (as shown).

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816